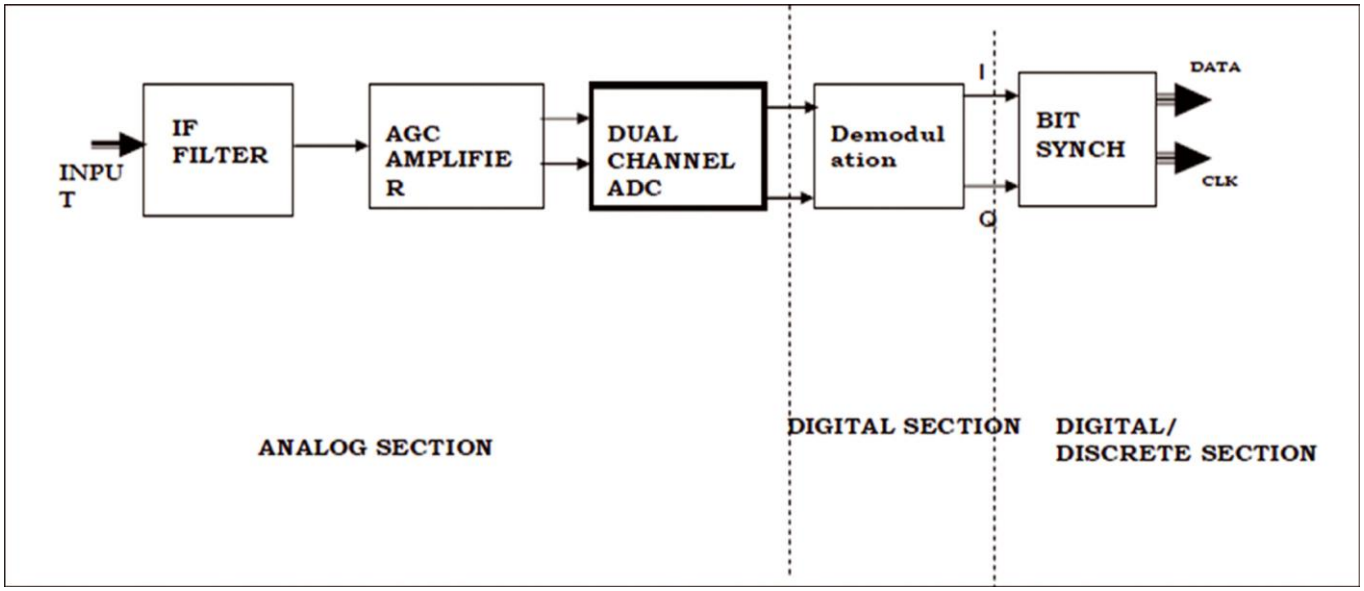
Design & Development of FPGA Based Digital Demodulator

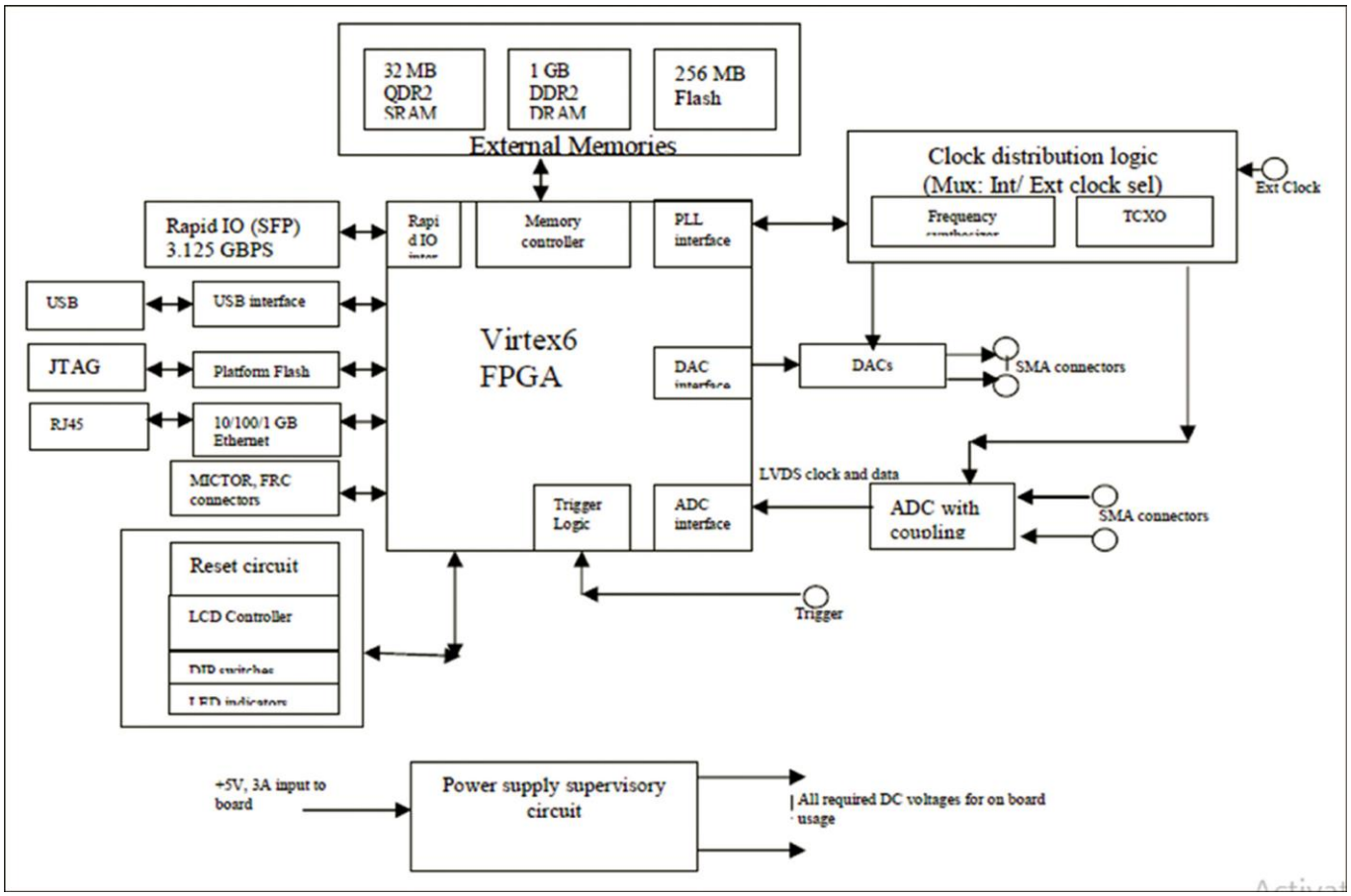
As different Satellites use different modulation schemes with variable data rates, in order to cater to the Multi-satellite data reception requirements of a ground station, it is necessary to have greater flexibility and programmability features embedded in the design of demodulators. The demodulation techniques for Binary/Quadrature Phase shift Keying (BPSK/ QPSK)are well established and understood when implemented with analog circuits. Recently, state-of-the-art digital technology allows Radio Frequency (RF) signals to be processed in the digital time domain. Modulated RF signals are digitally sampled and then demodulated in real-time using digital signal processing techniques implemented on FPGAs. Because of the usage of FPGAs, the design can have low power consumption, size and cost reduction. Furthermore, these digital demodulators can be reconfigured and upgraded to enhance the data rates in future.

The BPSK/ QPSK can be demodulate by different techniques such as squaring loop, Costas loop and others in analog domain. The Costas loop technique has adopted for developing the demodulator in digital domain as in this the carrier recovery and data demodulation can be done simultaneously with block level design. The high data rate digital demodulator is planned to perform IF amplification, filtering and analog to digital conversion of the received IF signal followed by a Digital demodulator. The basic design strategy includes a configurable data rate BPSK/ QPSK demodulation with COSTAS loop circuitry utilizing the flexibility of FPGA implementation.

The IP core development for the demodulation including carrier recovery have been tested for the 8 Mbps BPSK and 42.4515Mbps QPSK as shown in the block diagram. The Prototype Hardware implementation has done using separate ADC and FPGA evaluation board s. The final realization of the demodulator logic has implemented on an integrated ADC -FPGA board.



Block diagram of proposed demodulator



Block diagram of the final hardware with necessary interface circuitry

Specifications

Sampling frequency (Fs)	125 MHz-250 MHz
Carrier frequency	30 MHz (BPSK), 70 MHz (BPSK/QPSK)
Data Rates (Fb)	8 MBPS (BPSK), 42.4515 MBPS (QPSK)
Low pass filters used	Raised Cosine FIR
FIR sampling frequency	(Fs/10) for 8 MBPS datarateand (Fs/ 4) for 42.4515 MBPS data rate
FIR Cut-off frequency	1.5*(Fb/2) for BPSK and 1.5 * (Fb/ 4) for QPSK
Loop filter used	1st order Butter worth IIR
Loop filter cut-off frequency	200 KHz

Conclusion:

The design of demodulator is proven for 8MBPS data rate BPSK demodulation and 42.45 l 5MBPSQPSK demodulator and the test results are presented. The results show a promising inference for further scope of improvisation with respect to data rate and programmability.

Applications

- *High Data rate demodulation for remote sensing data reception system.*